In nanometer CMOS technologies, several new effects emerge, such as velocity saturation and gate leakage currents. As a result the transconductance and speed are both limited by velocity saturation. Also noise and mismatch are affected as a result of the thinner gate oxides used. Moreover the supply voltage is reduced to values below 1 Volt, creating new challenges for analog circuit design.

This presentation provides a review of the modifications in model parameters, including noise and distortion. It is followed by an exploration of the noise/power compromise in existing circuit blocks such as Miller operational amplifiers and Gm-C filters. An overview is given of low-voltage amplifiers/filters configurations with both Gate and Bulk drives. Several sub-1 Volt circuits are finally discussed for different applications.

Friday August 14 @ 3:00 PM
McGill University
McConnell Engineering Building, Room MC13
(refreshments served before the lecture)

Organizers:
Prof. M. Sawan, École Polytechnique de Montréal
Prof. Anas Hamoui, McGill University

Information: www.ieee.ece.mcgill.ca